FH1 Application Circuit at 240 MHz

Summary:

This application note details the operation and schematic of an application circuit using a WJ Communications FH1 device optimized for Noise Figure at 240 MHz, while providing high linearity (OIP3 = 42 dBm). This circuit is unconditionally stable and offers a gain of 17 dB with excellent input and output VSWR. The WJ Communications low-cost FET requires only single supply that can be sourced directly from a voltage regulator. This circuit is ideal for use as high linearity low-noise driver amplifiers for infrastructure equipment.

Frequency	240 MHz
S21 - Gain	16.9 dB
S11 - Input R.L.	-16.0 dB
S22 - Output R.L.	-27.5 dB
S12 - Isolation	-24.7 dB
Output IP3[1]	42 dBm
Noise Figure	1.75 dB
Bias	5 V at 150 mA

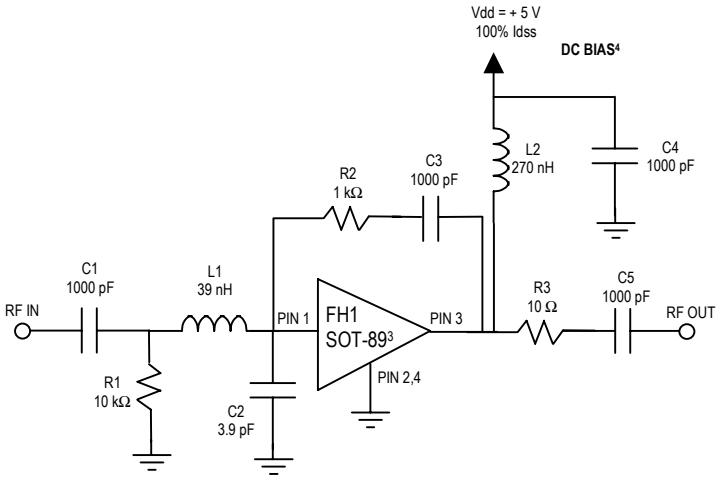


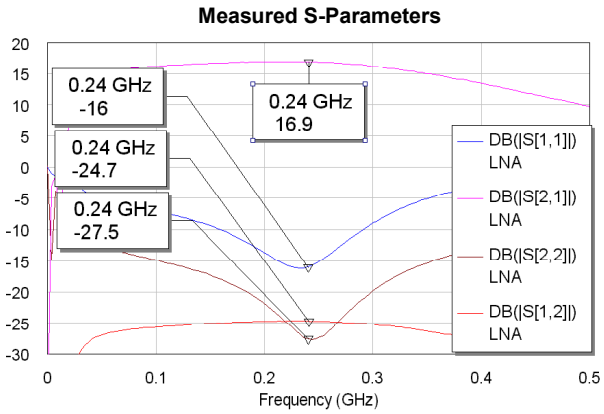
Fig 1. 240 MHz Circuit Schematic[2]

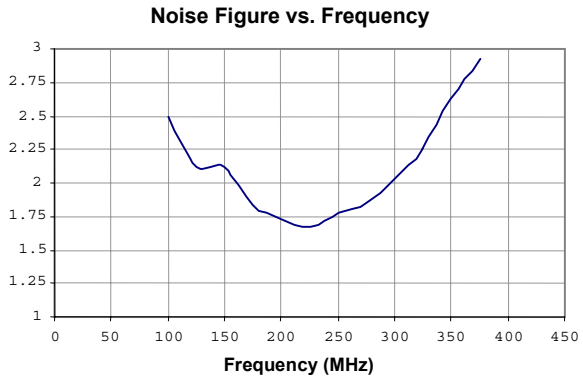
1 OIP3 is measured with 2 tones at an output power of 5 dBm/tone with 10 MHz spacing. The suppression on the largest IM3 product is used to calculate OIP3 using a 2:1 slope rule. Test parameters were taken at 25 °C.

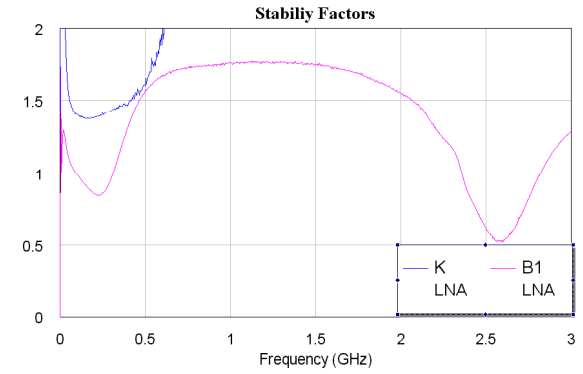
2 All components are 0603 size. All components can be standard 5% tolerance parts. Toko LL1608-FH chip inductors and AVX capacitors were used in the design.

3 The FET should be mounted as shown in the FH1 datasheet.

4 The application circuit should be biased directly into a constant voltage DC regulator. A dropping resistor is NOT required for biasing this device.







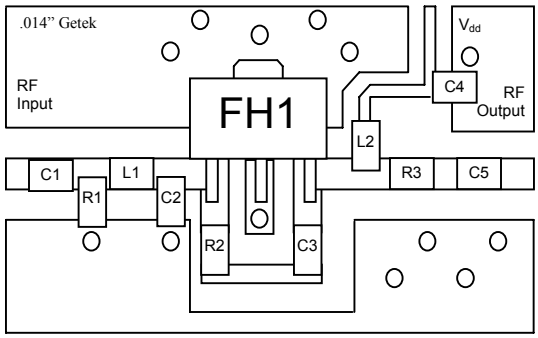


Fig. 2. 240 MHz Sample Board Layout